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Chemical Stability and Electrical Performance of Dual-Active-Layered Zinc–Tin–Oxide/Indium–Gallium–Zinc–Oxide Thin-Film Transistors Using a Solution Process

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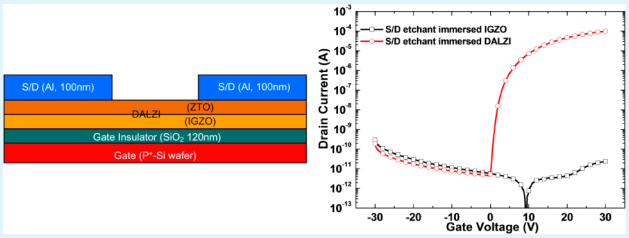
ABSTRACT: We investigated the chemical stability and electrical properties of dual-active-layered zinc–tin–oxide (ZTO)/indium–gallium–zinc–oxide (IGZO) structures (DALZI) with the durability of the chemical damage. The IGZO film was easily corroded or removed by an etchant, but the DALZI film was effectively protected by the high chemical stability of ZTO. Furthermore, the electrical performance of the DALZI thin-film transistor (TFT) was improved by densification compared to the IGZO TFT owing to the passivation of the pin holes or pore sites and the increase in the carrier concentration due to the effect of Sn^{4+} doping.



KEYWORDS: *thin-film transistors, dual-active-layered zinc–tin–oxide/indium–gallium–zinc–oxide, etch-stopper-layer, wet-etch, self-protection layer*

1. INTRODUCTION

Recent studies on amorphous indium–gallium–zinc–oxides (a-IGZO) as channel materials have focused on their role as substitutes for conventional amorphous silicon (a-Si) or polysilicon for the backplanes of next-generation active-matrix organic light-emitting diode (AMOLED) displays and active-matrix liquid-crystal displays (AMLCDs). The amorphous oxides have advantages such as high field-effect mobility, good uniformity, transparency in visible light, and compatibility with the conventional a-Si thin-film transistor (TFT) fabrication process. Moreover, the low-temperature deposition process of the IGZO thin film can be used to deposit channel materials on the bendable substrates used for flexible electronics.[1−5] In terms of fabrication process, IGZO thin film was easily damaged by its poor chemical stability under the metal etch process if the back-channel-etch (BCE) structure (Figure 1b) was employed. In order to protect the IGZO film surface from wet etch chemicals during the patterning of the source/drain (S/D) electrodes, it is essential to adopt the etch-stopper-layer (ESL) structure (Figure 1a) instead of the BCE structure. When compared to the BCE structure, the ESL structure has demerits such as a high cost, an additional lithography process (equivalent to requiring an additional design mask), and the existence of a large parasitic capacitance caused by the misalignment margin among the gate, ESL, and S/D.[6−11] Therefore, new processes and novel IGZO TFTs with BCE structures have been studied to develop TFTs that offer low cost and better electrical performance.[7,9]

Zinc–tin–oxide (ZTO) is one of the promising oxide-semiconductor materials for the channel region in a TFT. Even though ZTO has higher chemical stability than IGZO owing to its SnO_2 content, it is not widely used in the display industry compared to IGZO, which has high mobility and high reliability. In this study, we demonstrated fabrication of a simple BCE-based, chemically durable, dual-active-layered ZTO/IGZO (DALZI) TFT using a solution process. We devised the dual-active-layered structure using the IGZO thinfilm as the front-channel and the ZTO thinfilm as the back-channel. The IGZO front channel played the role of the main electron accumulation layer, while the ZTO thinfilm served as a protection layer to shield the IGZO thin film from conventional wet etchants used to form the S/D patterns. Furthermore, the ZTO thin film provides the contact resistance with the S/D electrodes for the switching device because it has the characteristics of a neutral degenerate semiconductor, compared with the high contact resistance of the ESL which has mainly an insulator property.[7,9,10] As a result, a DALZI TFT exposed to a wet etchant could show superior TFT performance without an ESL.

2. EXPERIMENTAL PROCEDURE

2.1. Preparation of IGZO and ZTO Solutions. A 0.1 M IGZO solution was synthesized by dissolving indium nitrate hydrate $[In(NO_3)_3{\cdot}xH_2O]$, gallium nitrate hydrate $[Ga(NO_3)_3{\cdot}xH_2O]$, and zinc nitrate hydrate $[Zn(NO_3)_2{\cdot}xH_2O]$ in 2-methoxyethanol as a solvent, with acetic acid as a stabilizer. The molar ratio of In:Ga:Zn was fixed at 3:1:2. After the IGZO solution was stirred for 1 h at 70 °C to form a homogeneous solution, it was passed through a 0.2 μm syringe filter and aged for over 24 h. A 0.15 M ZTO solution with a Zn:Sn molar ratio of 2:1 was prepared by dissolving zinc acetate dehydrate $[Zn(Ac)_2{\cdot}2H_2O]$ and tin(II) chloride $[SnCl_2]$ in 2-methoxyethanol. The stirring and filtering of the ZTO solution were performed under the same conditions as for the IGZO solution.

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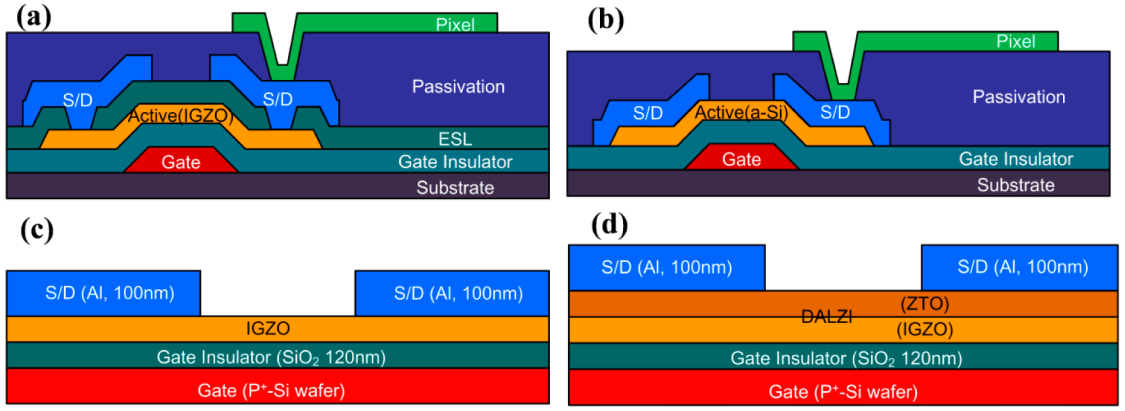

Figure 1. Schematic cross-section of the (a) ESL-structured IGZO TFT, (b) BCE-structured a-Si TFT, and the simple unpassivated BCE-structured (c) IGZO TFT and (d) DALZI TFT.

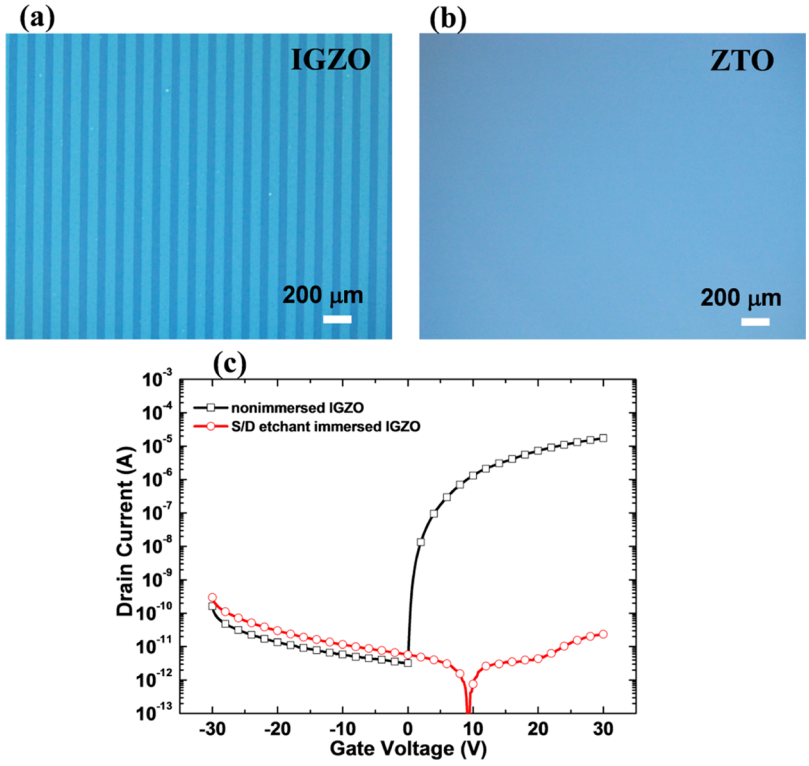

Figure 2. Optical microscopy image in plane view of (a) the immersed IGZO thin film and (b) the immersed ZTO thin film. (c) Transfer characteristic curves of the IGZO TFT as functions of the immersion process.

2.2. Device Fabrications. Schematics of the simple unpassivated BCE-structured IGZO TFT and DALZI TFT are shown in Figure 1c and d. For the fabrication of the IGZO TFT, an IGZO solution was spin-coated on a SiO_2 layer with a thickness of 120 nm (as the gate insulator), which was thermally grown on a heavily boron-doped Si wafer (as the gate electrode). The spin-coated thin film was prebaked at 300 °C in the air for 5 min to remove the solvent; it was then annealed at 450 °C in the air for 4 h. The as-annealed IGZO film had a thickness of about 10 nm. For the fabrication of the DALZI TFT, the ZTO thin film was formed with a thickness of about 20 nm on the IGZO thin film. Each layer of the DALZI TFT was annealed for 2 h, and the total annealing time was the same compared to the IGZO TFT.

To investigate the chemical durability of the IGZO thin film and the DALZI thin-film stack, we immersed the IGZO TFTs and the DALZI TFTs in an aluminum etchant (AL-11 with 72% phosphoric acid, 3% acetic acid, 3% nitric acid, and 22% water, Cyantek Co.) for 60 s at 50 °C. The etchant is used as a conventional etchant for patterning aluminum as S/D electrodes. Finally, aluminum S/D electrodes with a thickness of 100 nm were deposited on the S/D-etchant-immersed IGZO and DALZI structures via sputtering with a shadow mask. The channel area was defined with a channel width (W) of 1000 μm and a length (L) of 150 μm. The microstructural properties of the IGZO thin film and DALZI thin-film stack were analyzed via transmission electron microscopy (TEM) and optical microscopy (OM). The electrical properties of the films and TFTs were analyzed via Hall-effect measurements and the use of a semiconductor parameter analyzer in the dark at room temperature, respectively.

3. RESULTS AND DISCUSSION

3.1. The Chemical Stability of the IGZO and ZTO Layer. The IGZO thin film with the photoresist (PR) pattern was immersed in an aluminum etchant for 60 s at 50 °C. Figure 2a shows the OM image of the IGZO film surface after the PR pattern was removed. The immersed IGZO thin film provided

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an alternative way to study the effect of an aluminum etchant on IGZO as an exposed channel layer in the BCE structure during S/D patterning. Besides, 60 s is the time specified to etch the 900-nm-thick aluminum S/D and would be sufficient to etch the S/D used in conventional flat panel displays. Striped patterns of the IGZO thin film were formed owing to the poor chemical stability in an aluminum etchant, as shown in Figure 2a. However, the ZTO thin film was not changed by the aluminum etchant, as shown in Figure 2b, owing to the high chemical stability of SnO_2.[12] This result indicated that the ZTO layer could protect the IGZO layer from the conventional wet etchants used in S/D patterning. Figure 2c shows the transfer characteristic curves of the IGZO TFT as functions of aluminum etchant exposure before S/D deposition at a drain-to-source voltage (V_{DS}) of 10.1 V. The nonimmersed IGZO TFT showed normal switching behavior. However, the immersed IGZO TFT showed the only leakage current regardless of gate voltage value. This result suggested that the IGZO channel layer was fully etched by the aluminum etchant, and the IGZO TFT lost the switching capabilities.

3.2. Analysis on the Structure of DALZI Layer. Figure 3a shows the cross-sectional TEM image of the DALZI

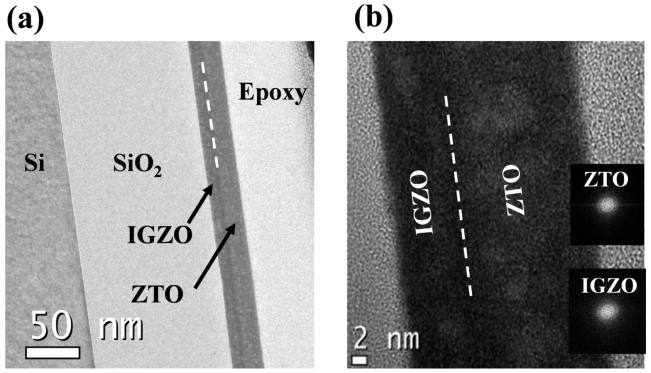

Figure 3. (a) Cross-sectional TEM image and (b) magnified high-resolution TEM image of the immersed DALZI thin-film stack. (Inset) SAED patterns of the IGZO and the ZTO thin film.

structure after it was immersed in an aluminum etchant for 60 s; a magnified high-resolution TEM image is shown in Figure 3b. No aggregation or defects at the interface between the IGZO and ZTO thin films were observed in the ZTO/IGZO stack on SiO_2, which suggested that the IGZO layer was protected by the ZTO layer despite the immersion process. In addition, the crystallinity of the IGZO and ZTO thin films was examined using selected area electron diffraction (SAED) patterns, as shown in the inset of Figure 3b. We could confirm that both IGZO and ZTO thin films were in the amorphous phase based on the broad, diffuse diffraction rings.

3.3. Electrical Characteristics of DALZI TFTs. Figure 4 shows the transfer characteristic curves of the IGZO- and DALZI-based TFTs under different immersion conditions before S/D deposition at a V_{DS} of 10.1 V. The nonimmersed DALZI TFT and the immersed DALZI TFT showed field-effect mobilities (μ_{FE}) of 2.09 and 1.97 $cm^2/V{\cdot}s$, threshold voltages (V_{TH}) of 2.72 and 3.94 V, and subthreshold swings (SS) of 0.49 and 0.58 V/decade, respectively (as listed in Table 1). The DALZI TFT retained its switching properties regardless of the immersion process compared to the IGZO TFT, indicating that the ZTO layer provided good protection from damage by the aluminum etchant. When comparing the

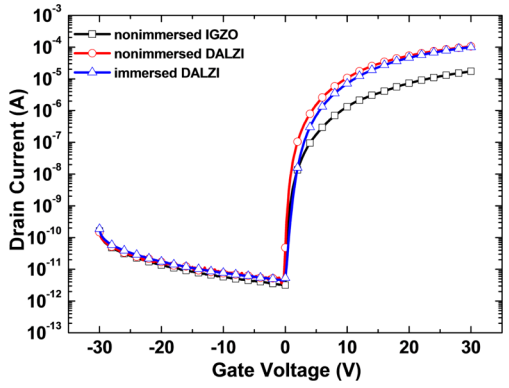

Figure 4. Transfer characteristic curves of the IGZO and DALZI TFTs as functions of the immersion process.

Table 1. Comparison of Device Parameters of the IGZO and DALZI TFTs as a Function of the Immersion Process

device structure	μ_{FE} ($cm^2/(V\ s)$)	V_{TH} (V)	SS (V/decade)
nonimmersed IGZO	0.32	4.43	0.55
immersed IGZO		no active	
nonimmersed DALZI	2.09	2.72	0.49
immersed DALZI	1.97	3.94	0.58

characteristics of the nonimmersed IGZO TFT and the immersed DALZI TFT (Table 1), the immersed DALZI TFT showed even better electrical performances.

We assumed two probabilities of the improved device characteristics. The first could be attributed to passivation of the porous IGZO thin film, including the large numbers of pin holes and pore sites. Solution-processed oxide films usually have low density and high porosity. However, stacking the ZTO thin film on top of the IGZO thin film could passivate the pin holes or pore sites as a result of the penetration of Zn and Sn atoms in the liquid phase.[15,16] In the second, the improved characteristics could be attributed to the doping behavior of Sn^{4+} ions that replaced the In^{3+}, Ga^{3+}, or Zn^{2+} ions in the IGZO thin film, which could determine the overall DALZI TFT performance due to its location directly adjacent to the TFT gate dielectric, during annealing of the spin-coated DALZI stack. In other words, the Sn^{4+} ions acted as cationic dopants in the IGZO lattice and served as substitutes for indium, gallium, or zinc. In In_2O_3, Ga_2O_3, and ZnO, since the metal ions had valences of two and three, the Sn ions acted as *n*-dopants of the IGZO lattice by providing electrons to the conduction band.[26−30] Therefore, the electrical conductivity of the DALZI structure was increased, supported by the larger carrier concentration (1.34×10^{16} cm^{-3}) of the immersed DALZI thin-film stack compared to that (1.47×10^{15} cm^{-3}) of the nonimmersed IGZO thin film obtained through hall measurements. We found slight degradation of the immersed DALZI TFT compared to the nonimmersed DALZI TFT. The carrier concentration of the nonimmersed DALZI thinfilm was also measured as 1.46×10^{16} cm^{-3}. This result indicates that the immersed DALZI layer was slightly damaged rather than perfectly immune by the aluminum etchant.

3.4. Bias Stability of DALZI TFTs. To investigate the effect of the ZTO thin film serving as a protection layer on the bias stability of the DALZI TFTs in terms of the instability of the oxide semiconductor TFT,[23−25] the positive bias stress (PBS) was performed at a V_{GS} = 20 V and a V_{DS} = 10.1 V. The maximum stress duration was 1000 s. Unpassivated IGZO

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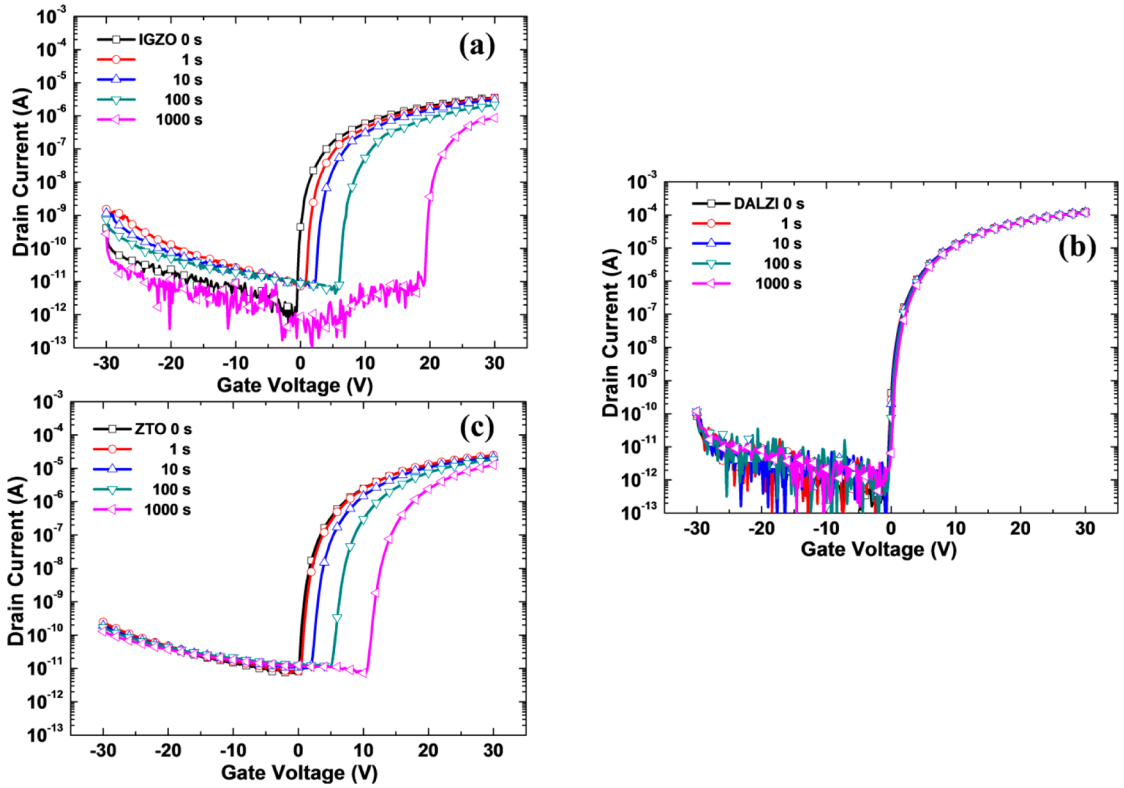

Figure 5. Transfer characteristic curves of (a) IGZO, (b) DALZI, and (c) ZTO TFT as functions of the applied stress time.

TFTs with the same active layer thickness of DALZI were fabricated using a 0.3 M IGZO solution considering the effect of active layer thickness on the bias stability.[17−19] Figure 5a and b show the transfer curves as a function of the applied stress time for the unpassivated IGZO TFT and DALZI TFT, respectively. The positive shift in V_{TH} without significant change in μ_{FE} was founded. The unpassivated IGZO TFT showed a large V_{TH} shift of 19.2 V (from 0.5 to 19.7 V), while a V_{TH} shift of the DALZI TFT was very small at 0.6 V. The superior stability of the DALZI TFT could be attributed to not only the reduction of trap sites by the passivation of the porous IGZO thin film due to the stacked-ZTO but also the middle-interface formed by the stacked-DALZI structure between the IGZO and ZTO layer. Previous papers have reported that the middle-interface capturing free electron contributed to weakening of the electric filed under gate voltage stress.[15,21,33] Therefore, the DALZI TFT has good stability under the PBS due to the decrease in the interaction between the exposed back surface and oxygen in ambient atmosphere, as well as the reduction of trap sites.[22] The PBS stability of the unpassivated single layer ZTO (0.15 M) TFT for confirming the effect of the upper layer ZTO on the stability of the DALZI TFT is shown in Figure 5c. The stress condition is the same as that of the IGZO and DALZI TFT. The positive shift in V_{TH} of the ZTO TFT was smaller than that of the IGZO TFT but much larger than the DALZI. This result indicates that the improved stability of the DALZI TFT was not caused by the ZTO layer alone but by the advantage of the stacking process in the solution process.

4. CONCLUSION

In summary, we investigated the chemical stability and electrical properties of IGZO and DALZI films and TFTs with the simple unpassivated BCE structure instead of the ESL structure. We found that the ZTO layer in the DALZI structure offered many advantages, including the following properties: (1) protection of the IGZO channel layer from an aluminum S/D etchant, (2) densification of the IGZO channel layer owing to the passivation of the pin holes or the pore sites, (3) an increase in the carrier concentration owing to the doping behavior of Sn^{4+}, and (4) support of the superior stability under the PBS due to the densification of the IGZO channel. Although the active patterning of DALZI could be considered to have difficulty due to the low sensitivity of wet etching of the ZTO layer, this problem could be resolved by using a common etchant of IGZO and ZTO such as oxalic acid.[31,32] Therefore, the DALZI structure with the self-protection layer of the chemical damage would ultimately lead to high-performance oxide TFTs with BCE structures.

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Author Contributions

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Notes

The authors declare no competing financial interest.

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